In th Claims

Claims 1-4 (cancelled)

Claim 5 (currently amended): A method of forming circuitry comprising the following steps:

providing a substrate, the substrate including a semiconductor material;

defining a memory array region of the substrate and an other region of the substrate spaced from the memory array region; said other region comprising a conductively-doped region of the semiconductor material ~~a peripheral region of the substrate, the peripheral region being peripheral to the memory array region~~;

forming a capacitor construction over the memory array region of the substrate, the capacitor construction comprising a pair of capacitor electrodes spaced from one another by at least a dielectric layer and a first barrier layer ~~a storage node, a capacitor dielectric layer, a capacitor barrier layer and a cell plate layer; the capacitor dielectric layer separating the storage node from the cell plate layer, the capacitor barrier layer separating the capacitor dielectric layer from one of the storage node and the cell plate~~;

forming an electrical interconnect over ~~the peripheral region~~ said other region of the substrate and in electrical connection with the conductively-doped region ~~a doped region~~, the electrical interconnect comprising a ~~conductive interconnect~~ second barrier layer over the conductively-doped region and a metal layer over the second barrier layer~~, the conductive interconnect barrier layer being between the doped region and the metal layer~~; and

wherein the ~~conductive interconnect barrier layer and capacitor~~ first and second barrier layers are formed in a same step.

Claim 6 (currently amended): The method of claim 5 wherein the ~~capacitor barrier layer and conductive interconnect barrier layer~~ first and second barrier layers comprise TiN.

Claim 7 (currently amended): The method of claim 5 wherein the ~~capacitor barrier layer and conductive interconnect barrier layer~~ first and second barrier layers comprise TiN, and wherein the same step comprises chemical vapor deposition.

Claim 8 (currently amended): The method of claim 5 wherein the ~~capacitor barrier layer and conductive interconnect barrier layer~~ first and second barrier layers comprise TiN, and wherein the metal layer comprises one or more of Ti, W, Al and Cu.

Claims 9-12 (cancelled).

Claim 13 (currently amended): A method of forming circuitry, comprising:

providing a substrate which comprises a semiconductive material;

defining a memory array region of the substrate and ~~a peripheral~~ an other region of the substrate spaced from the memory array region~~, the peripheral region being peripheral to the memory array region~~;

~~defining~~ providing a first electrical node ~~proximate~~ associated with the memory array region of the substrate, and ~~defining~~ providing a second electrical node ~~proximate~~ associated with said other ~~the peripheral~~ region of the substrate;

~~forming an electrically insulative layer over the substrate and over the electrical nodes;~~

~~forming a first opening through the electrically insulative layer;~~

forming a first capacitor electrode ~~at least a portion of a capacitor storage node within the first opening and~~ in electrical connection with the first electrical node;

~~forming a second opening through the electrically insulative layer to the second electrical node;~~

in a common deposition step, forming a conductive material over the ~~storage node~~ first capacitor electrode and ~~within the second opening~~ in electrical connection with the second electrical node; and

forming a capacitor dielectric layer ~~and a capacitor electrode operatively adjacent the storage node~~ and a second capacitor electrode over the first capacitor electrode to form a capacitor construction comprising the capacitor dielectric layer and the first and second capacitor electrodes, one of the ~~storage node or the capacitor electrode~~ first and second capacitor electrodes comprising the conductive material.

Claim 14 (currently amended) The method of claim 13 ~~further~~ comprising:

forming ~~a first~~ an electrically conductive layer over the ~~storage node layer~~ first capacitor electrode and over the ~~insulative layer before etching the second opening~~ second electrical node prior to the common deposition step; ~~and~~

etching an ~~the second~~ opening through the ~~first~~ electrically conductive layer to the second electrical node; and

wherein the common deposition step forms the conductive material within the opening.

Claim 15 (currently amended): The method of claim 14 wherein the ~~first~~ electrically conductive layer comprises at least one of TiN and WN.

Claim 16 (currently amended): The method of claim 14 wherein the ~~first~~ electrically conductive layer comprises TiN.

Claim 17 (currently amended): The method of claim 14 further comprising forming the capacitor dielectric layer over the ~~storage node layer~~ first capacitor electrode before forming the ~~first~~ electrically conductive layer.

Claims 18-22 (cancelled).

Claim 23 (currently amended): The method of claim 13 wherein the ~~substrate~~ semiconductive material comprises monocrystalline silicon and the electrical nodes comprise electrically conductive diffusion regions formed within the ~~substrate~~ semiconductive material.

Claim 24 (currently amended): The method of claim 13 wherein the forming the conductive material comprises forming a metal-comprising layer ~~over the storage node layer and within the second opening~~.

Claim 25 (currently amended): The method of claim 13 wherein the forming the conductive material comprises forming at least two layers ~~over the storage node layer and within the second opening~~.

Claim 26 (currently amended): The method of claim 13 wherein the forming the conductive material comprises forming at least three layers ~~over the storage node layer and within the second opening~~.

Claim 27 (currently amended): The method of claim 13 wherein the forming the conductive material comprises:

forming a layer comprising TiN ~~over the storage node layer and within the second opening~~; and

forming a second layer over the layer comprising TiN, the second layer not comprising TiN.

Claims 28-45 (cancelled).

Claim 46 (new): The method of claim 5 where the first and second barrier layers are together part of a common and continuous layer.